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Per my conversation with Joel, four dis-similar paragraphs from the MOSIS web site, to prime the distiller.

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The Scalable CMOS (SC) rules support both n-well and p-well processes. MOSIS recognizes three base technology codes that let the designer specify the well type of the process selected. SCN specifies an n-well process, SCP specifies a p-well process, and SCE indicates that the designer is willing to utilize a process of either n-well or p-well. An SCE design must provide both a drawn n-well and a drawn p-well; MOSIS will use the well that corresponds to the selected process and ignore the other well. As a convenience, SCN and SCP designs may also include the other well (p-well in an SCN design or n-well in an SCP design), but it will always be ignored.
MOSIS currently offers only n-well processes or foundry-designated twin-well processes that from the design and process flow standpoints are equivalent to n-well processes. These twin-well processes may have options (deep n-well) that provide independently isolated p-wells. For all of these processes at this time use the technology code SCN. SCP is currently not supported, and SCE is treated exactly as SCN.

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This CMOS process has 6 metal layers and 1 poly layer. The process is for 1.8 volt applications. A thick oxide layer can be used for 3.3 volt transistors. MOSIS multiproject runs support designs for the 0.18 micron CMOS logic process (CL018) using epitaxial wafers, and mixed signal/RF process (CM018) using non-epitaxial wafers.

Silicide block, thick gate oxide (3.3 V), NT_N, deep n_well, ThickTopMetal (inductor), and MiM options are available on multiproject runs. The Thick_Top_Metal option must be explicitly specified with each design submission that requires it. MiM (Cap_Top_Metal, also known as Metal 5 Prime, to Metal 5) provides a capacitance of 1 fF/μm^2. Designs for this process require Metal 6 in the pad stack.

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For processes that provide a "thick oxide" option (for operation at voltages above the standard process voltage), the MOSIS Thick_Active layer selects which active areas receive the thick gate oxide. Active by itself will have the standard process thin (gate) oxide. Active overlapped by Thick_Active will have the thicker gate oxide. Thick_Active by itself does nothing. Anything outside Active (regardless of whether Thick_Active is present or not) gets field oxide.

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Each university (domestic or foreign) must have a MOSIS Customer Agreement executed by an individual empowered to enter into a legal agreement on behalf of the university. This agreement includes a Non-Disclosure Agreement (NDA) that is legally binding to both the university and the faculty, the students and the staff who have access to MOSIS vendor proprietary material. Failure to honor the terms of the NDA can lead to litigation against the university and against individuals who have access to these documents. The procedures MOSIS is implementing are intended to increase awareness of the legal issues of proprietary material access.

A professor can be accepted as a signatory only upon receipt by MOSIS of a statement from the university legal department on university letterhead acknowledging the authority of said professor to enter into a legal agreement on behalf of the university.

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